

WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device, comprising:  
providing a semiconductor substrate;  
forming a first insulating layer over the semiconductor substrate;  
forming a floating gate over the first insulating layer with a reaction gas,  
wherein the floating gate comprises a microcrystalline material having a grain size of about 50-300Å;  
forming a second insulating layer over the floating gate; and  
forming a control gate over the second insulating layer.
2. The method of claim 1, wherein the first insulating layer comprises an oxide, a nitride, or a combination thereof.
3. The method of claim 1, wherein the second insulating layer comprises an oxide, a nitride, or a combination thereof.
4. The method of claim 1, wherein the floating gate is formed with a combination of the reaction gas and a second gas.
5. The method of claim 4, wherein the reaction gas comprises SiX, wherein X comprises at least one of H<sub>4</sub>, H<sub>2</sub>Cl<sub>2</sub>, HCl<sub>3</sub>, D<sub>4</sub>, D<sub>2</sub>Cl<sub>2</sub>, and D<sub>3</sub>Cl.

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6. The method of claim 4, wherein the reaction gas comprises SiX, Si<sub>2</sub>Y, or a combination of SiX and Si<sub>2</sub>Y.

7. The method of claim 6, wherein X comprises at least one of H<sub>4</sub>, H<sub>2</sub>Cl<sub>2</sub>, HCl<sub>3</sub>, D<sub>4</sub>, D<sub>2</sub>Cl<sub>2</sub>, and D<sub>3</sub>Cl.

8. The method of claim 6, wherein Y comprises at least one of H<sub>6</sub>, H<sub>4</sub>Cl<sub>2</sub>, H<sub>2</sub>Cl<sub>4</sub>, D<sub>6</sub>, D<sub>4</sub>Cl<sub>2</sub>, and D<sub>2</sub>Cl<sub>4</sub>.

9. The method of claim 4, wherein the second gas comprises one or more of D<sub>2</sub>, H<sub>2</sub>, and D<sub>3</sub>.

10. The method of claim 1, further comprising forming a plurality of bit lines in the semiconductor substrate.

11. The method of claim 1, further comprising forming a layer of nitride over the control gate layer.

12. The method of claim 1, further comprising thermally treating the floating gate to increase the grain size of the microcrystalline material to about 200-600Å.

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13. A method of forming a semiconductor device, comprising:

- providing a silicon substrate;
- selective doping of the silicon substrate to form a plurality of bit lines in the silicon substrate;
- forming a first insulating layer over the silicon substrate;
- forming a floating gate over the first insulating layer, wherein the floating gate comprises an amorphous material;
- thermally treating the memory cell to transform the amorphous material into a microcrystalline material;
- forming a second insulating layer over the floating gate; and
- forming a control gate over the second insulating layer.

14. The method of claim 13, wherein the grain size of the microcrystalline material is about 200-500Å.

15. The method of claim 13, wherein the step of forming the floating gate further comprises depositing the floating gate with a combination of gases, wherein the combination of gases comprise a reaction gas.

16. The method of claim 15, wherein the reaction gas comprises SiX, Si<sub>2</sub>Y, or a combination of SiX and Si<sub>2</sub>Y, wherein X comprises at least one of H<sub>4</sub>, H<sub>2</sub>Cl<sub>2</sub>, HCl<sub>3</sub>, D<sub>4</sub>, D<sub>2</sub>Cl<sub>2</sub>, and D<sub>3</sub>Cl, and Y comprises at least one of H<sub>6</sub>, H<sub>4</sub>Cl<sub>2</sub>, H<sub>2</sub>Cl<sub>4</sub>, D<sub>6</sub>, D<sub>4</sub>Cl<sub>2</sub>, and D<sub>2</sub>Cl<sub>4</sub>.

17. The method of claim 15, wherein the step of forming the floating gate further comprises depositing the floating gate with a combination of the reaction gas and a second gas comprising at least one of D<sub>2</sub>, H<sub>2</sub>, and D<sub>3</sub>.

18. The method of claim 13, further comprising forming a layer of nitride over the control gate.

19. A method of forming a semiconductor memory device, comprising:  
providing a semiconductor silicon substrate;  
forming a plurality of bit lines in the silicon substrate;  
depositing a first insulating layer over the silicon substrate including the plurality of bit lines;  
forming a floating gate over the first insulating layer, wherein the floating gate comprises one of amorphous material or a microcrystalline material having a grain size of 50-300Å;  
forming a second insulating layer over the floating gate;  
forming a plurality of word lines over the second insulating layer; and  
forming a layer of nitride over the plurality of word lines.

20. The method of claim 19, further comprising thermally treating the floating gate so that the floating gate has a grain size of about 200-500Å.

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